

## CLAIMS

What is claimed is:

- 1        1.        An apparatus, comprising:  
2                a content addressable memory (CAM) array;  
3                an output register coupled to the CAM array, the output register  
4        configured to output data based on a delayed clock signal; and  
5                a programmable delay circuit coupled to receive a reference clock  
6        signal and generate the delayed clock signal using a delay element.
  
- 1        2.        The apparatus of claim 1, wherein the programmable delay circuit  
2        comprises:  
3                a plurality of the delay elements to generate a plurality of delayed  
4        clock signals;  
5                a programmable register to store information indicating a  
6        particular delayed clock signal of the plurality of delayed clock signals;  
7        and  
8                a multiplexer coupled with the programmable register and the  
9        plurality of delay elements to select the particular delayed clock signal  
10       based on the information.
  
- 1        3.        The apparatus of claim 2, wherein the programmable delay circuit  
2        further comprises a decoder coupled to the programmable register to  
3        decode the information stored in the programmable register.

1        4.        The apparatus of claim 2, wherein each of the plurality of delay  
2        elements provides a different time period of delay to the reference clock  
3        signal.

1        5.        The apparatus of claim 4, wherein one of the plurality of delay  
2        elements provides substantially a zero time period of delay.

1        6.        The apparatus of claim 4, wherein at least one of the plurality of  
2        delay elements comprises a series of inverters.

1        7.        The apparatus of claim 1, wherein the reference clock signal is  
2        received at a clock pad and wherein the programmable delay circuit is  
3        coupled between the clock pad and the output register.

1        8.        The apparatus of claim 7, further comprising a second  
2        programmable delay circuit coupled between the first programmable  
3        delay circuit and the output register.

1        9.        The apparatus of claim 8, wherein the programmable delay circuit  
2        and the second programmable delay circuit each comprise a separate  
3        programmable register.

1        10.       The apparatus of claim 7, further comprising an instruction  
2        decoder coupled to the clock pad to receive the reference clock signal.

1        11.       The apparatus of claim 2, wherein the information for the  
2        programmable register indicates the particular delayed clock signal  
3        according to a frequency of the reference clock signal.

1        12.    The apparatus of claim 1, wherein the programmable delay circuit  
2        is a first programmable delay circuit comprising:  
3                a first plurality of the delay elements to generate a first plurality of  
4        delayed clock signals;  
5                a first programmable register to store first information indicating a  
6        first particular delayed clock signal of the first plurality of delayed clock  
7        signals; and  
8                a first multiplexer coupled with the first programmable register  
9        and the first plurality of delay elements to select the first particular  
10       delayed clock signal based on the first information, and wherein the  
11       apparatus further comprises a second programmable delay circuit  
12       coupled with the first programmable delay circuit.

1        13.    The apparatus of claim 12, wherein the second programmable  
2        delay circuit comprises:  
3                a second plurality of the delay elements to receive the first  
4        particular delayed clock signal and generate a second plurality of delayed  
5        clock signals;  
6                a second programmable register to stored second information  
7        indicating a second particular delayed clock signal of the second plurality  
8        of delayed clock signals; and  
9                a second multiplexer coupled with the second programmable  
10       register and the second plurality of delay elements to select the second  
11       particular delayed clock signal based on the second information.

- 1 14. The apparatus of claim 12, wherein the second programmable  
2 delay circuit comprises:  
3 a second plurality of the delay elements to receive the first  
4 particular delayed clock signal and generate a second plurality of delayed  
5 clock signals, the first programmable register for storing second  
6 information indicating a second particular delayed clock signal of the  
7 second plurality of delayed clock signals; and  
8 a second multiplexer coupled with the first programmable register  
9 and the second plurality of delay elements to select the second particular  
10 delayed clock signal based on the second information.
- 1 15. The apparatus of claim 7, further comprising a processor coupled to  
2 the clock pad to transmit the reference clock signal.
- 1 16. The apparatus of claim 1, further comprising a processor coupled  
2 with the output register to receive the data.
- 1 17. The apparatus of claim 1, further comprising a read circuit coupled  
2 between the CAM array and the output register.
- 1 18. The apparatus of claim 1, wherein the CAM array comprises a  
2 plurality of rows of CAM cells each having a corresponding match line.
- 1 19. The apparatus of claim 18, further comprising a match flag circuit  
2 coupled to the match lines and the output register.
- 1 20. The apparatus of claim 18, further comprising an encoder circuit  
2 coupled to the match lines and the output register.

- 1        21.    An apparatus, comprising:  
2                a content addressable memory (CAM) array;  
3                a clock circuit coupled to the CAM array; and  
4                a programmable delay circuit coupled to receive a reference clock  
5                signal and generate a programmable delayed clock signal using a  
6                delay element for the clock circuit.
- 1        22.    The apparatus of claim 21, wherein the programmable delay circuit  
2                comprises:  
3                    a plurality of the delay elements to generate a plurality of delayed  
4                clock signals;  
5                    a programmable register to store information indicating a  
6                particular delayed clock signal of the plurality of delayed clock signals;  
7                and  
8                    a multiplexer coupled with the programmable register and the  
9                plurality of delay elements to select the particular delayed clock signal  
10              based on the information.
- 1        23.    The apparatus of claim 22, wherein the programmable delay circuit  
2                further comprises a decoder coupled to the programmable register to  
3                decode the information stored in the programmable register.
- 1        24.    The apparatus of claim 22, wherein each of the plurality of delay  
2                elements provides a different time period of delay to the reference clock  
3                signal.

- 1        25.    The apparatus of claim 21, wherein the clocked circuit comprises a  
2        read circuit for reading data from the CAM array.
- 1        26.    The apparatus of claim 21, wherein the clocked circuit comprises a  
2        register for storing comparand data for comparison with data of the CAM  
3        array.
- 1        27.    The apparatus of claim 21, wherein the CAM array comprises a  
2        plurality of rows of CAM cells each having a corresponding match line for  
3        carrying a match signal indicative of whether comparand data matches  
4        data of the corresponding row of CAM cells.
- 1        28.    The apparatus of claim 27, wherein the clocked circuit comprises an  
2        encoder circuit coupled to the match lines and the programmable delay  
3        circuit.
- 1        29.    The apparatus of claim 28, wherein the clocked circuit comprises  
2        match flag logic coupled to the match lines and the programmable delay  
3        circuit.
- 1        30.    The apparatus of claim 21, further comprising:  
2                a second clocked circuit; and  
3                a second programmable delay circuit.
- 1        31.    An integrated circuit device configured to operate based on a  
2        reference clock signal, comprising:  
3                a clock pad to receive the reference clock signal;

4           a programmable delay circuit coupled to receive the reference clock  
5           signal and generate a delayed clock signal using at least one delay  
6           element; and  
7           an output register configured to output data based on the delayed  
8           clock signal.

1           32.    The integrated circuit device of claim 31, wherein the  
2           programmable delay circuit comprises:  
3                a plurality of the delay elements to generate a plurality of delayed  
4           clock signals;  
5                a programmable register to store information indicating a  
6           particular delayed clock signal of the plurality of delayed clock signals;  
7           and  
8                a multiplexer coupled with the programmable register and the  
9           plurality of delay elements to select the particular delayed clock signal  
10          based on the information.

1           33.    The integrated circuit of claim 32, wherein the programmable delay  
2           circuit further comprises a decoder coupled to the programmable register  
3           to decode the information stored in the programmable register.

1           34.    The integrated circuit of claim 32, further comprising a second  
2           programmable delay circuit coupled between the programmable delay  
3           circuit and the output register.

1 35. The integrated circuit of claim 34, wherein the programmable delay  
2 circuit and the second programmable delay circuit each comprise a  
3 separate programmable register.

1 36. The integrated circuit of claim 32, wherein the information for the  
2 programmable register indicates the particular delayed clock signal  
3 according to a frequency of the reference clock signal.

1 37. A method, comprising:  
2 receiving a reference clock signal;  
3 generating a delayed clock signal based on the reference clock  
4 signal using programmed information representing a value of a delay  
5 time period; and  
6 outputting data based on the delayed clock signal.

1 38. The method of claim 37, wherein the reference clock signal is  
2 received by a content addressable memory (CAM) device and the delayed  
3 clock signal is generated internally in the CAM device.

1 39. The method of claim 37, wherein the delayed clock signal is  
2 generated without feedback between the delayed clock signal and the  
3 reference clock signal.

1 40. The method of claim 37, further comprising generating the delayed  
2 clock signal using a second programmed information representing the  
3 value of second delay time period.

1       41.    The method of claim 37, further comprising programming the  
2       programmed information.

1       42.    The method of claim 40, further comprising programming the  
2       second programmed information based on an anticipated frequency of  
3       operation for the reference clock signal.

1       43.    A method, comprising:  
2                establishing a connection with a register in a content addressable  
3       memory (CAM) device; and  
4                programming the register in the content addressable memory  
5       (CAM) device with information representing a value of a delay time  
6       period for the generation of a delayed clock signal.

1       44.    The method of claim 43, further comprising:  
2                generating the delayed clock signal based on a reference clock  
3       signal using the programmed information; and  
4                outputting data based on the delayed clock signal.

1       45.    The method of claim 44, further comprising:  
2                programming the register with additional information representing  
3       the value of another delay time period; and  
4                generating the delayed clock signal using the additional  
5       information.

1       46.    The method of claim 44, further comprising:

2 programming a second register with second information  
3 representing the value of a second delay time period; and  
4 generating the delayed clock signal using the second information.

1 47. The method of claim 46, further comprising programming the  
2 second programmed information based on an anticipated frequency of  
3 operation for the reference clock signal.

1 48. An apparatus, comprising:  
2 means for receiving a reference clock signal;  
3 means for generating a delayed clock signal based on the reference  
4 clock signal using programmed information representing a value of a  
5 delay time period; and  
6 means for outputting data based on the delayed clock signal.

1 49. The apparatus of claim 48, further comprising means for generating  
2 the delayed clock signal using additional programmed information  
3 representing the value of second delay time period.

1 50. The apparatus of claim 49, further comprising means for  
2 programming the second programmed information based on an  
3 anticipated frequency of operation for the reference clock signal.

1 51. An apparatus configured to operate based on a reference clock  
2 signal, comprising:  
3 a content addressable memory (CAM) array;  
4 means for generating a delayed clock signal using at least one delay  
5 element in response to the reference clock; and

6 a clocked circuit coupled to receive the delayed clock signal.

1 52. The integrated circuit device of claim 51, wherein the means for  
2 generating comprises means for generating the delayed clock signal using  
3 first and second programmed information representing values of first and  
4 second delay time periods, respectively.

1 53. The integrated circuit device of claim 52, further comprising means  
2 for programming the second programmed information based on an  
3 anticipated frequency of operation for the reference clock signal.